\[ \Delta \psi \approx 1.4^\circ \] which is 20 times larger than the result previously reported by us [14].

The search for a wider AED was also attempted choosing \( \mathbf{E}^\text{dc} \) parallel to \(-\hat{z}, \hat{x} \cos \psi + \hat{z} \sin \psi, \text{and } -\hat{x} \sin \psi + \hat{z} \cos \psi\) for the same choices of \( n \) and \( \chi \) values. But we could get only \( \Delta \psi \) of order 0.02\(^\circ\). However, we wish to continue the search hoping for wider AED.

3. CONCLUDING REMARKS

In summary, DSWs propagate along interfaces involving birefringent materials over a narrow angular range \( \Delta \psi \) of the orientation angle \( \psi \). Having a larger \( \Delta \psi \) is helpful for easier generation and detection of DSWs. Several attempts have been made to widen this AED. By considering specific directions of an applied dc electric field and specific values of \( \chi \), we have shown that exploitation of the linear electro-optic (Pockels) effect has the potential to widen the AED. The search for higher values of \( \Delta \psi \) for an arbitrarily oriented dc electric field is still open. Also, one might look into ranges of \( \chi \) values for specific values of \( \psi \) and various magnitudes and directions of the applied dc electric field.

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where \( R_L \) and \( R_C \) are the series resistance of the inductor and capacitance of the tank, respectively.

\( R_O \) is the total output impedance of cross-coupled transistor [2].

To achieve the low power consumption, the \( R_{p,tot} \) in Eq. (1) needs to be maximized. The resistance of the tank can be maximized, by maximizing the inductance and quality factor. But, when we use the inductor in the design kit supported from the selected process, the quality factor is limited at around 13. Thus, if the circuit makes the low parasitic capacitance, which leads to select the maximum inductance, the low power consumption might be achieved.

From this point of view, to select the small-sized switch in the coarse tuning branch and the small-sized varactor will make the low parasitic and guide the current consumption low. To reduce the off-capacitance of coarse-tuning branch, the scheme in Figure 3 is employed.

2.2. \( K_{vco} \) Linearizer

A-MOS (Accumulation MOS) varactor is employed as a variable capacitor dependent on a bias voltage. In Figure 5, the capacitance variation slope of conventional varactor is too high around the center voltage of \( V_{ctrl} \) [2]. Because the high slope makes the high gain of VCO, this makes the phase noise of the PLL system worse. Additionally, the useful range of \( V_{ctrl} \) is so narrow, only from 0.4 to 0.8 V.

To solve this entanglement, we employed multireference bias scheme at the gate of varactor, as shown in Figure 4. The transfer functions of three different biased varactors are summed and the final simulated results are shown in Figure 5. If this linearizer is used, the \( K_{vco} \) gain of VCO, is linear according to control voltage and decreased by about 50%. The useful range of the control voltage of that is increased to near VDD. If this VCO is implemented in the PLL system, the phase noise performance might be improved, because of the lowered \( K_{vco} \).

Figure 1 Block diagram of LO generator

Figure 2 Schematic of designed VCO

Figure 3 Schematic of individual coarse-tuning branch

Figure 4 Schematic of \( K_{vco} \) linearizer with multi-reference bias
2.3. Low-Power Buffer Design

To drive the passive type mixer, the around 800 mVpp signal swing should be generated from LO generator. So, the inverter type amplifier in Figure 6 is employed to make the high gain and consume the low power.

To block the current spiking, the capacitor, C1, is used. The maximum current is limited by the current mirror, compared with the conventional inverting amplifier without current source.

The single input from the test pin needs to be converted to the differential signal to drive internal circuits, as shown in Figure 7. In high frequency operation, the mismatch in differential conversion can be compensated by crossed connection of mirroring (M5–M8). The differential and symmetric swing by following push–pull connection (M9–M16) can be achieved.

3. MEASUREMENT RESULTS

The measured oscillation frequency according to control voltage and selected coarse band is plotted in Figure 8. The transfer curve looks like linear curve within 0.0–1.2 V control voltage and the oscillation frequency changes 1.0–1.7 GHz with 49% tuning range. The measured gain of VCO is 64.6–213.7 MHz/V.

In Figure 9, VCO consumes 600 and 400 μA with the measured phase noise of $-120$, and $-116$ dBc/Hz at 1-MHz offset in L5 band (1176.45 MHz) and L1 band (1572.42 MHz), respectively. The measured performance is summarized in Table 1.

The VCO buffer, PLL buffer, and mixer buffer in Figure 1 consume 400, 300, and 400 μA, respectively. Because the bidirectional buffer is turned off during normal operation and turned on during only for testing, this current can be ignored. The total circuit draws around 1.7–1.9 mA from 1.2 V power supply.

To evaluate the overall performance, a figure-of-merit (FOM) is used, which is given by
TABLE 1 Measured VCO and LO Generator Performance Summary

<table>
<thead>
<tr>
<th>Technology</th>
<th>Operating band</th>
<th>VDD</th>
<th>Current dissipation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1P8M 0.13-μm CMOS</td>
<td>L5 (1.18 GHz)</td>
<td>1.2 (V)</td>
<td>VCO core (600 μA)</td>
</tr>
<tr>
<td></td>
<td>L1 (1.57 GHz)</td>
<td></td>
<td>VCO core (400 μA),</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VCO buffer (400 μA),</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PLL buffer (300 μA)</td>
</tr>
<tr>
<td>Tuning range</td>
<td>1–1.7 GHz (49%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VCO gain</td>
<td>64.6 MHz/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PN @ 1 MHz</td>
<td>120 dBc/Hz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>116 dBc/Hz</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

FOM = 10 log \( \frac{kT f_o}{P (f_{o,\text{max}} - f_{o,\text{min}})} \) − PN(Δf),

where \( f_o \) is the carrier frequency, \( \Delta f \) is the offset frequency, \( P \) is the power consumed by the VCO core, and PN(Δf) is the phase noise measured at the offset Δf from the carrier.

4. CONCLUSION

A complementary CMOS VCO is implemented, which is optimized to lower power consumption without degradation of phase noise performance. The \( K_{\text{vco}} \) linearizer is effective to lower VCO gain and obtain linear frequency controllability according to the control voltage without reducing tuning range, which leads to 50% reduction in the gain of the VCO. The current-limited high gain buffer and bidirectional buffer in the LO generator, fully compliant with receiver performance, are implemented. The total power consumption of LO generator is about 2 mW with 1000 μm × 615 μm area in 0.13-μm 1P8M CMOS process, as shown in Figure 10.

Table 2 shows how this number compares to some other notable published VCOs. In 1.57 GHz, the FOM is best compared with others, but in 1.18 GHz, the FOM is worse, because of high power consumption and low gain.


5. W. Cheng, C. Chan, K. Pun, and C. Choy, 0.8V GPS band CMOS VCO with 29% tuning range, Presented at the IEEE APCCAS, 2006.


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BROADBAND DIGITAL PHASER BASED ON COMPOSITE RIGHT/LEFT-HANDED TRANSMISSION LINE

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ABSTRACT: The broadband digital phase shifter is valuable for modern phase array antennas. Under balanced condition, composite right/left-handed transmission line (CRLH TL) is broadband because of its unique hyperbolic-linear dispersion relations. A broadband 4-bit digital phase shifter based on the broadband property of CRLH TL is designed. When the absolute error is less than ±5°, for the 180° stage of the phase shifter, the relative bandwidth achieves 31.3%, while the conventional 180° switched line phase shifter only achieves 8.9%. And the unique hyperbolic-linear dispersion relations are also able to minimize the area of the phase shifter. A simple circuit to test the right-handed (RH) effect of the left-handed (LH) TL is fabricated and used successfully in the design process of the 4-bit digital phase shifter. The simulation and experiment results show that the design method of the phase shifter is feasible. © 2008 Wiley Periodicals, Inc. Microwave Opt Technol Lett 50: 2365–2368, 2008; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.23665

Key words: composite right/left-handed transmission line; phase shifter; broadband; hyperbolic-linear dispersion; right-handed effect

1. INTRODUCTION

In recent years, LH metamaterials, which have found many possible uses in electromagnetics and optics fields, gradually become a research hotspot in the high technology fields. However LH bulk metamaterials are not easy to be fabricated, and at present the man-made LH metamaterials in the laboratories are of large loss and narrowband [1]. In the case of it, Eleftheriades [2, 3], Oliner [4], and Caloz [5, 6] etc. proposed the transmission line theory to analyze LH metamaterials, respectively. Among them, Caloz [7] etc. proposed composite right/left-handed transmission line theory, analyzed CRLH TL systematically, and summarized some characteristics of CRLH TL, such as dual-band, broadband, miniaturization, zeroth order resonance, etc. Noticeably, this type of transmission line may be made of not only lumped elements but also distributed elements, which makes CRLH TL have good application prospects in the microwave circuits.

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2. W. Cheng, C. Chan, K. Pun, and C. Choy, 0.8V GPS band CMOS VCO with 29% tuning range, Presented at the IEEE APCCAS, 2006.

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